cadence®

CDNLive! EMEA 2011

3-5 May

Dolce Hotel Munich, Germany

cdn LIVE EMEA 2011

Agenda

Tuesday 3rd May, 2011

12:00	Registration Opens					
12:00 - 13:30	Light Lunch Buffet					
	Silicon Realization - Unified Custom/ Analog Flow Design	Silicon Realization - Functional Verification	Silicon Realization - Unified Digital Flow	Silicon Realization - PCB & IC Packaging	Soc Realization - MEMCON	System Realization
13:30 - 15:30	Techtorial 13:30 Comparison of Different Modeling Approaches to Assist the Mixed-Signal RF Top-Level Simulation and Functional Verification 14:45 How to boost Mixed-Signal Design Implementation Productivity	Techtorial Universal Verification Methodology (UVM) 1.0	Techtorial Take on Giga-Gate/ GHz, Low-Power, and Mixed-Signal Design Challenges Using the Cadence 28nm-Ready Unified Digital Flow	Techtorial 1. Introduction of the new DDR3 Design-In Kit 2. PDN (Power Delivery Network Analysis) with 16.5 Allegro PCB SI	MEMCON Techtorial Choosing and Designing Low-power Memory Interfaces	Techtorial (Invitation Only - Please contact your local sales representative)
15:30 - 16:00	Coffee Break					
16:00 - 17:45	Techtorial (continued 16:45 In-Design Signoff Verification	Functional Verification Techtorial continued	United Digital Flow Techtorial continued	PCB & IC Packaging Techtorial continued	MEMCON Techtorial continued	System Realization - Techtorial continued
17:45 - 20:00	Networking Buffet and Refreshments					

Wednesday 4th May, 2011

07:30 - 08:30	Breakfast & Registration (Foyer)					
08:30 - 08:40	Introduction					
8:40 - 9:20	Cadence Keynote					
9:20 - 10:00	Industry Keynote					
10:00 - 10:30	Coffee Break					
	Silicon Realization - Unified Custom/ Analog Flow Design	Silicon Realization - Functional Verification	Silicon Realization - Unified Digital Flow	Silicon Realization - PCB & IC Packaging	SoC Realization - MEMCON	Academic Track
10:30 - 11:00	CD01 Top-level simulation and functional verification of the RFDAC based multi-standard transmitter RWTH Aachen	FV01 Roadmap	DI01 Hierarchical low power flow for the ARM Mali-400 MP GPU Cadence	PCB01 OrCAD Marketplace overview Cadence/Flowcad	MEM01 Breaking Down the Memory Wall Through Innovation Micron	AC01 Lead institution for Dependability and Design for Testability: An introduction Delft University of Technology

Wednesday, 4th May, 2011 (continued)

	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging	SoC Realization: MEMCON	Academic Track
11:00 - 11:30	CD02 Mixed-Signal Simulation experience with Multi-Chip Module Design Texas Instruments	FV02 Roadmap	DI02 How database access commands can make your life easier Freescale Semiconductor	PCB02 What's new in OrCAD 16.5 Cadence/Flowcad	MEM02	AC02 Lead institution for Digital Design Automation: An introduction Polytechnico di Torino
11:30 - 12:00	CD03 VCOs Simulation using Spectre RF NXP	FV03 Roadmap	DI03 ETS AOCV handeling statistical variabilities Texas Instruments	PCB03 What's new in Allegro 16.5 Cadence/Flowcad	MEM03	AC03 Lead institution for Advanced SoC Verification Techniques:TBA University of Heidelberg
12:00 - 13:00	Lunch / Designer Expo / Canvas Conversations					

	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging	Silicon Realization: PCB & IC Packaging	SoC Realization: MEMCON	Academic Track
13:00 - 13:30	CD04 Roadmap	FV04 Using ESL models in functional verification Siemens	DI04 Close data gaps between flows using basic features of Conformal CDC Freescale Semiconductor	PCB04 Allegro SPB Module Design Velux As	PCB09 What's new in OrCAD/Allegro Front-end 16.5 (Capture, DE-HDL, ASA, FSP, PSpice, ADW) Cadence/Flowcad	MEM04 Roadmap	AC04 Partner Presentations Partners
13:30 - 14:00	CD05 Roadmap	FV05 FlexRayTM Conformance Testing using OVM Verilab	DI05 Implementation strategies for a high performance Cortex-A15 Arm Holdings	PCB05 Behavioral Modeling facilitates Chip-Package Codesign Mohagi LLC	PCB09 What's new in OrCAD/Allegro Front-end 16.5 (Capture, DE-HDL, ASA, FSP, PSpice, ADW) Cadence/Flowcad	MEM05 Roadmap	AC05 Implementation of a Post-Layout Optimization method with Automatic Device Type Selection within practical analog circuit design processes IMMS GmbH
14:00 - 14:30	CD06 Roadmap	FV06 Advanced ***e*** Language Debugging - An IDE Perspective AMIQ Consulting	DI06 Migrating a Front-End Flow to RTL Compiler, and Application to a 28nm Wireless IP Texas Instruments	PCB06 Advances in Creepage and Air Gap Analysis in Electro-mechanical Products with NEXTRA Mecadtron	PCB10 What's new in OrCAD/Allegro PCB 16.5 Cadence/Flowcad	MEM06 Roadmap	AC06 IC Design Activities in the Microelectronics Students' Group Faculdade de Engenharia da Universidade do Porto
14:30 - 15:00	Coffee Break						

Wednesday, 4th May, 2011 (continued)

	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging English Track	Silicon Realization: PCB & IC Packaging English/German Track	SoC Realization	System Realization	Educational Services
15:00 - 16:00	Unified Custom/ Analog Flow design demo 1	Functional Verification demo 1	Unified Digital Flow demo 1	15:00-15:30 PCB07 Collaborative Mechatronics Engineering: Mastering product development complexity and improving design efficiency Dassault Systemes 15:30-16:00 PCB08 Simplified Workflow for Full 3D Simulation in Cadence SiP Flow using CST STUDIO SUITE 2011- CST AG	PCB11 What's new in OrCAD/Allegro PCB 16.5 Cadence/ Flowcad	SoC Realization demo 1	System Realization demo 1	Educational Services demo 1
16:00 - 17:00	Unified Custom/ Analog Flow design demo 2	Functional Verification demo 2	Unified Digital Flow demo 2	Orcad Marketplace Touch and feel event	Orcad Marketplace Touch and feel event	SoC Realization demo 2	System Realization demo 2	Educational Services demo 2
17:00 - 18:15	Designer Expo							
18:15 - 23:00	Evening Event at the Dolce							

Thursday, 5th May, 2011

7:30 - 8:30	Breakfast						
	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging English/ German Track	Silicon Realization: PCB & IC Packaging German Track	System Realization	Academic Track
8:30 - 9:00	CD07 Design of a Continuous-Time Sigma-Delta Modulator for Bluetooth KTH Electrum	FV07 DMS as quality improvement for complex mixed signal power management designs Texas Instruments	DI07 Logic Equivalence Checking is not always logical and may not be equivalent Freescale Semiconductor	PCB12 What's new in Allegro IC Packaging & SiP Cadence/Flowcad	PCB12 What's new in Allegro IC Packaging & SiP Cadence/Flowcad	SDV01 Roadmap	AC07 Physical Implementation of Analog Circuits Assisted by Conventional Digital Place and Route Methods - Electrical and Information Technology (EIT), Lund University

Thursday, 5th May, 2011 (continued)

	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging English/ German Track	Silicon Realization: PCB & IC Packaging German Track	System Realization	Academic Track
9:00 - 9:30	CD08 Mastering mixed signal IC with Cadence Encounter Digital Implementation STMicroelectronics	FV08 Speeding up the development of register assertions by re-using functionality from an interface Freescale Semiconductor	DI08 Low-Power Design Challenges: An Implementation Perspective Imec	PCB13 Allegro 16.5 NEW Product Packaging Cadence/Flowcad	PCB13 Allegro 16.5 NEW Product Packaging Cadence/Flowcad	SDV02 Roadmap	AC08 Development of Mixed Signal Design Kits and Workflows to improve design productivity of ASICs for applications on large scale Particle Physics - Cern
9:30 - 10:00	CD09 Overlapping timing verification at the interface of Custom and Digital Design Infineon	FV09 Successfully Migrating SoC Verification Environments into the UVM Library Freescale Semiconductor	DI09 Important ECOs implementation using gate-array-like mask configurable cells STMicroelectronics	PCB13 Allegro 16.5 NEW Product Packaging Cadence/Flowcad	PCB13 Allegro 16.5 NEW Product Packaging Cadence/Flowcad	SDV03 Roadmap	AC09 Systematic Design of OpAmps using Cadence ADE XL Technical University of Cluj-Napoca
10:00 - 10:30	Coffee Break						
10:30 - 11:00	CD10 DEF File Export Considering Overlapping Structures IFTE, TU Dresden	FV10 Keeping Bugs From Being Checked-in With Automated Change Management Technology Cadence	DI10 Roadmap	PCB14 Allegro/OrCAD Roadmap	PCB14 Allegro/OrCAD Roadmap	SDV04 Design Flow for High Level Synthesis of Digital Signal Processing Algorithms from Simulink Models Politecnico Di Torino	AC10 Implementation of an RF-DAC based multistandard transmitter system IAS RWTH Aachen
11:00 - 11:30	CD11 Advancements in Reliability Simulation Cadence + Robert Bosch GmbH	FV11 Experiences in Developing and Using OVM and UVM VIP Test and Verification Solutions	DI11 Roadmap	PCB14 Allegro/OrCAD Roadmap	PCB14 Allegro/OrCAD Roadmap	SDV05 SoC Architecture Analysis with ARM Fast Models Arm Holdings	AC11 Apprentices and Masters on MSE Level Fachhochschule Nordwestschweiz
11:30 - 12:00	CD12 Enabling advanced IC6.1 features and flows using X-FAB design kits XFAB	FV12 UVM Low Power Cadence	DI12 Roadmap	PCB14 Allegro/OrCAD Roadmap	PCB14 Allegro/OrCAD Roadmap	SDV06 Using ISX GDB Server for Software Debugging on a Simulated STMicroelectronics Processor STMicroelectronics	AC12 Cadence Tools in the Context of Side-Channel Attacks - Institute for Applied Information Processing and Communications (IAIK), Graz University of Technology
12:00 - 12:30	CD13 SiGe MEMS Process Design Kit from MEMS-IC Design - Coventor	FV13 Developing a generic and configurable testbench to verify different CPU architectures NoBug Consulting	DI13 Implementation Aspects of a 3D Architecture Cadence	PCB17 What's new in OrCAD/Allegro Signal & Power Integrity Cadence	PCB18 Tutorial - What's new in OrCAD / Allegro Front end 16.5 Flowcad	SDV07 ISX HW-SW co-verification challenges on a 16-bit microcontroller system Texas Instruments	AC13 The Application of Layout Module Generators upon Circuit Structure Recognition Reutlingen University / RBZ

Thursday, 5th May, 2011 (continued)

	Silicon Realization: Unified Custom/ Analog Flow Design	Silicon Realization: Functional Verification	Silicon Realization: Unified Digital Flow	Silicon Realization: PCB & IC Packaging English/ German Track	Silicon Realization: PCB & IC Packaging German Track	System Realization	Academic Track
12:30 - 13:00	CD14 Industry Needs a New Mixed Signal Design and Sign-Off Simulation Flow Texas Instruments	FV14 Verification Efficiency, Quality, and Productivity Through Consistency Broadcom	DI14 Overview: A Standard Cell Development flow for new Technology/ PDK Turn On GLOBALFOUNDRIES	PCB17 What's new in OrCAD/Allegro Signal & Power Integrity Cadence	PCB18 Tutorial - What's new in OrCAD / Allegro Front end 16.5 Flowcad	SDV08 Protocol analysis for PCI Express for Cadence 360 LeCroy	AC14 Electro-migration check with Cadence Virtuoso I2it
13:00 - 14:30	Lunch and Best Paper Presentations						
14:00 - 16:00					PCB19 Tutorial - What's new in OrCAD / Allegro PCB Editor 16.5 Flowcad		
16:00 - 17:00					PCB20 Tutorial - What's new in OrCAD / Allegro PCB 16.5 (Auto Routing, Constraint Manager) Flowcad		