cadence®

Delivering on the EDA360 Vision

A first-year report from Cadence

"Today, systems and semiconductor companies are undergoing a disruptive transformation so profound that even the best-known companies will be impacted. The EDA industry now stands at a crossroads where it also must change in order to continue as a successful, independent business. Without that change, EDA will become a fragmented industry offering suboptimal, poorly targeted solutions that fail to solve customer problems. As a result, the huge leap forward provided by the electronics revolution will come to a standstill."

– *EDA360: The Way Forward for Electronic Design* (April 2010)

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In 2010, Cadence® outlined a new vision for the electronic design automation (EDA) industry called EDA360. It was a response to a disruptive transformation that's visible everywhere—the emergence of software applications, or "apps," as the primary differentiator for electronic products.

As the competitive focus shifts to "apps," systems companies are increasingly expecting their semiconductor suppliers to provide not only silicon, but embedded software as well. Many systems companies expect semiconductor providers to supply complete hardware/software platforms ready for applications development and deployment.

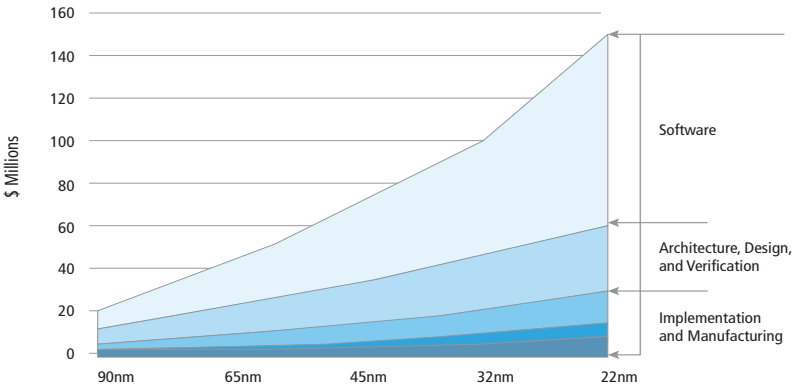

Figure 1: IC design costs are accelerating at advanced process nodes. Source: IBS

This demand for these hardware/software platforms is causing a crisis for the semiconductor companies at the worst possible time. Silicon complexity is skyrocketing, time-to-market is shrinking, and development costs are going through the roof. On top of that, many semiconductor companies now employ more software engineers than hardware engineers. As shown in the chart, system-on-chip (SoC) development costs at the 22nm node are expected to reach to $140 million, with over half the cost attributed to software.

To confront cost and time-to-market challenges, semiconductor companies are shifting their emphasis from design creation to design integration using silicon intellectual property (IP). The EDA industry has historically ignored design integration and focused on IP creation. However, integrators have different needs from creators. While still supporting design creation—in fact, vastly improving it—the EDA360 vision calls for new tools, methodologies, and IP sources for integrators.

How can EDA enable the new era of application-driven electronics? The answer lies in the three "Realizations" that underlie the EDA360 vision.

System Realization is the development of a complete hardware/software platform that will provide all necessary support for end-user applications. System Realization includes the architecture, design, integration, and verification of complex systems. These capabilities must be delivered through offerings that are *open* (based on industry standards and open formats), *connected* (integrated for easy migration between different levels of abstraction), and *scalable* (capable of meeting performance and capacity needs).

SoC Realization refers to the creation of an individual SoC. It includes design IP, services, and tools and methodologies for the architectural exploration, integration, and verification of complex SoCs. Design IP offerings need to be *differentiated* (focused on high-value IP), *integrated* (including PHY, controller, verification IP, software drivers, and services) and *proven* (shown to work in silicon).

Silicon Realization represents everything it takes to get a design into packaged silicon. The end result could be analog, digital, or mixed-signal IP for SoC integration; a complete IP subsystem; or an entire IC without embedded software. Silicon Realization provides the design, verification, and implementation of complex designs across silicon, package and board. It requires end-to-end flows that provide unified design *intent*, appropriate use of design *abstraction*, and *convergence* into a solution that meets the original specification.

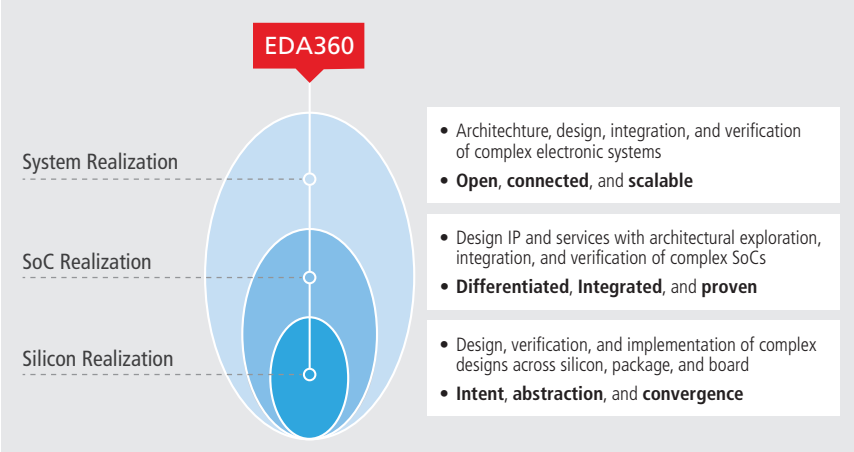

Figure 2: The EDA360 vision is based on three "Realizations."

While EDA360 is a vision for the entire industry, this "year one" report focuses on how Cadence has delivered on the vision from April 2010 to May 2011. It summarizes several types of developments—corporate re-alignments, product and technology announcements, and customer and partner engagements. All of the developments reported here have been publicly announced by Cadence, and further information is available at the Cadence.com web site. The following table provides a quick overview of company, product, and technology announcements.

Announcement	Silicon Realization	SoC Realization	System Realization	Customer/ Partner Endorsements
April 2010				
Palladium XP Verification Computing Platform			•	Nvidia
May 2010				
Cadence Acquires Denali	•	•	•	
August 2010				
Cadence Realigns R&D Organizations	•	•	•	
October 2010				
Holistic Flows Support Silicon Realization	•			
January 2011				
Silicon Realization Boosts Verification Productivity	•			Teradyne
End-to-End Digital Flow Extends to 28 nm	•			Global Unichip
February 2011				
Cadence Extends Verification IP Catalog	•	•	•	
March 2011				
First Wide I/O Memory IP Announced		•		
Unified Custom/Analog Flow Supports System Realization	•			Wolfson Microelectronics
April 2011				
First DDR4 IP Solution		•		
New Allegro Technology Supports Three Realizations	•	•	•	Thales Aerospace
May 2011				
Cadence System Development Suite			•	Nvidia, ARM
Cadence Acquires Altos Design Automation	•			
OrCAD Capture Marketplace	•			

Corporate Alignments

Since the release of the EDA360 vision paper, Cadence completed two acquisitions and an internal restructuring in support of EDA360.

Cadence Acquires Denali (completed June 2010)

In May 2010, Cadence announced its intention to acquire Denali Software, a leading provider of design IP, verification IP (VIP), and memory models. The $315 million acquisition, completed in June, immediately placed Cadence at the center of the growing IP market. Cadence and Denali expertise and IP was brought together to create expanded, industry-leading design IP and VIP portfolios, giving Cadence a strong position in SoC and System Realization.

Following the Denali acquisition, Cadence set forth a comprehensive SoC Realization strategy that includes chip planning tools, IP integration services, and design IP. In April 2011, leveraging over 10 years of technology experience at Denali, Cadence announced the industry's first DDR4 IP solution (described in more detail below). Denali expertise is also behind the Cadence announcement of the first wide I/O memory controller IP in March 2011.

Cadence Realigns R&D Organizations (August 2010)

Further demonstrating its commitment to EDA360, Cadence realigned its entire R&D operation in August 2010 around the EDA360 "Realizations." The company set up System Realization, SoC Realization, and Silicon Realization R&D groups. Today these R&D groups are focusing on integrated solutions based on EDA360 concepts.

Cadence Acquires Altos Design Automation (May 2011)

Altos Design Automation developed leading-edge technology that enables foundation IP development for the delivery of complex SoCs at advanced nodes. The acquisition of Altos boosts the Cadence Silicon Realization portfolio with tools that provide rapid characterization of memory, standard cell libraries, and other IP.

Product and Technology Announcements

Over the past year Cadence made a number of announcements that support System Realization, SoC Realization, and Silicon Realization. Major announcements are listed in chronological order below.

Palladium XP Verification Computing Platform (April 2010)

Figure 3: Palladium XP Verification Computing Platform

The Cadence Palladium® XP Verification Computing Platform is a key element of the Cadence System Realization strategy. This computing platform unifies simulation, RTL acceleration, and emulation into a single verification environment, with the ability to "hot swap" simulation with acceleration and emulation. With sufficient speed to run software drivers and applications, and SpeedBridge adapters that connect to real-world hardware, the Verification Computing Platform allows hardware/software integration using real-world scenarios with RTL hardware accuracy.

Today the Verification Computing Platform is a key element in the Cadence System Development Suite, a connected set of four hardware/software development platforms that was announced May 2011.

Holistic Flows Support Silicon Realization (Oct. 2010)

Cadence announced a number of product enhancements aimed at creating holistic Silicon Realization flows for analog and digital design. The enhancements reinforce the three principal requirements of Silicon Realization—unified design intent, abstraction, and convergence. Here are a few examples:

- Unified design intent – analog, physical and electrical constraints can drive digital content into mixed-signal flows, and vice versa.
- Abstraction – designers can create die abstracts for IC/package co-design and 3D-IC development.
- Convergence – new physical, electrical, and functional links between logic design, verification, and implementation allow rapid engineering change orders (ECOs).

At the time of this announcement, Cadence also published a detailed whitepaper that explained how unified design intent, abstraction, and convergence work within end-to-end Silicon Realization flows.

Silicon Realization Boosts Verification Productivity (Jan. 2011)

Bringing Silicon Realization principles to functional verification, Cadence rolled out a number of new capabilities that help engineers achieve faster verification closure through unified intent, abstraction, and convergence. For example, to leverage verification intent, engineers can now merge coverage data from formal analysis and simulation into a unified verification plan. Additional abstraction capabilities facilitate early bug detection, and faster verification engines speed verification convergence. A key part of the release was support for the Accellera Universal Verification Methodology (UVM), a standard that may eventually address all three EDA360 "Realizations."

New End-to-End Digital Flow Extends to 28nm (Jan. 2011)

Providing a deterministic path to silicon down to 28nm, Cadence announced a Silicon Realization digital IC design flow based on the Encounter® Digital Implementation System. The flow includes numerous technology enhancements that support unified intent, abstraction, and convergence. Here are a few examples:

- Unified design intent – silicon-proven 28nm design rule intent (including electrical, physical, and manufacturability) supports up-front tradeoff analysis.
- Abstraction – new technology allows large blocks of logic to be modeled simply and accurately, and optimized across logical and physical domains.
- Convergence – in-design signal-integrity and timing analysis tools facilitate convergence within the design flow.

This announcement also included an integrated 3D-IC design flow spanning digital, full custom, and package design.

Cadence Extends Verification IP Catalog (Feb. 2011)

Cadence combined verification IP (VIP) developed by Denali with VIP developed at Cadence to create a VIP Catalog that supports more than 30 complex and emerging protocols. Further, the entire portfolio works with third-party simulators and the Universal Verification Methodology. New use models include system validation with accelerated VIP that addresses hardware/software integration. Cadence VIP thus supports System Realization as well as SoC Realization and Silicon Realization.

Unified Custom/Analog Flow Supports Silicon Realization (March 2011)

Custom/analog design has been a Cadence strength since the company's inception in 1988, and in 2011 Cadence rolled out a unified flow based on Silicon Realization requirements. Based on the Cadence Virtuoso® platform, the flow brings a holistic approach to analog, custom digital, RF, and mixed-signal design, implementation and verification. Key features of the flow include:

- Unified intent – built-in design checking software maintains design intent in globalized work forces.
- Abstraction – "parasitic-aware design" makes it possible to estimate parasitics prior to extraction, and to bring this information back to schematic designers.
- Convergence – "in design" analysis engines within the Virtuoso environment help eliminate lengthy signoff iterations.

The unified flow is part of the new Virtuoso IC 6.1.5 release.

First DDR4 IP Solution (April 2011)

The Cadence DDR4 IP solution, the first available for this emerging memory standard, includes hard and soft PHY, controller, memory models, VIP, tools and methodologies. It also comes with signal-integrity reference designs for the package and board. This announcement leveraged years of DDR technology development at Denali.

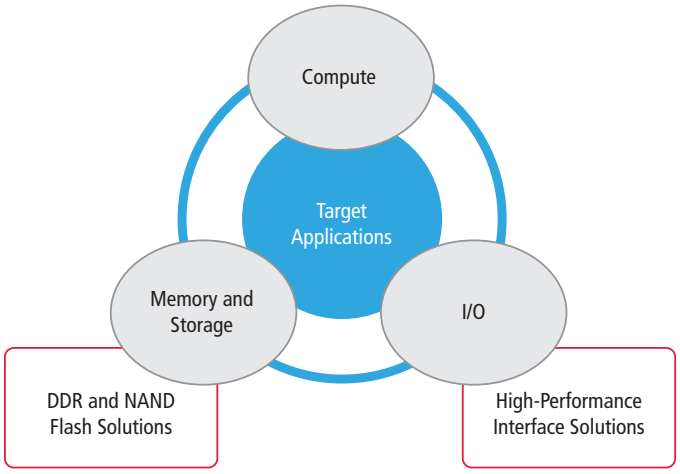

Figure 4: The Cadence SoC Realization strategy places a strong emphasis on memory and storage controller IP.

At the time of this announcement, Cadence also defined a comprehensive SoC Realization strategy that includes chip planning tools, IP integration services, and design IP. From an IP standpoint, the strategy is as follows:

- Leverage years of technology development at Denali and within Cadence Services to provide a broad suite of memory and storage IP.
- Focus on high-performance, differentiated interface IP, such as PCI Express Gen3 as well as 10/40 Gigabit Ethernet.
- Collaborate with companies such as ARM to provide proven processor IP.

New Cadence Allegro Technology Supports All Three "Realizations" (April 2011)

A new release of the Cadence Allegro® PCB and IC packaging tools, Allegro 16.5, illustrates how this toolset offers features that support System Realization, SoC Realization, and Silicon Realization. It also reinforced the importance of package and board design in the overall EDA360 vision. Here's how the new release supports each of the three "Realizations":

- **System Realization**: power is a system-wide problem, and the Power Delivery Network (PDN) feature in Allegro 16.5 helps analyze power problems that show up at the board level.
- **SoC Realization**: Cadence DDR3 design IP now comes with a Design-In Kit that ensures signals are going to work across the package and board.
- **Silicon Realization**: a new "distributed" IC/package co-design capability allows teams to exchange an abstracted, XML definition of a chip. Design intent is represented by pinouts, parasitics, and netlists, and convergence occurs as a package-optimized chip is successfully taped out.

The OrCAD Capture Marketplace, announced May 2011, provides an on-line "apps" store that helps users take a design from concept to final board realization.

Cadence System Development Suite (May 2011)

The Cadence System Development Suite represents a major leap towards System Realization. It provides a set of four integrated hardware/software development platforms that support hardware/software co-development from the architectural level through final prototyping. The suite provides an offering that is open (based on industry standards), connected (allowing fast migration between platforms), and scalable (able to meet needs for capacity, performance and high-volume distribution of software development platforms).

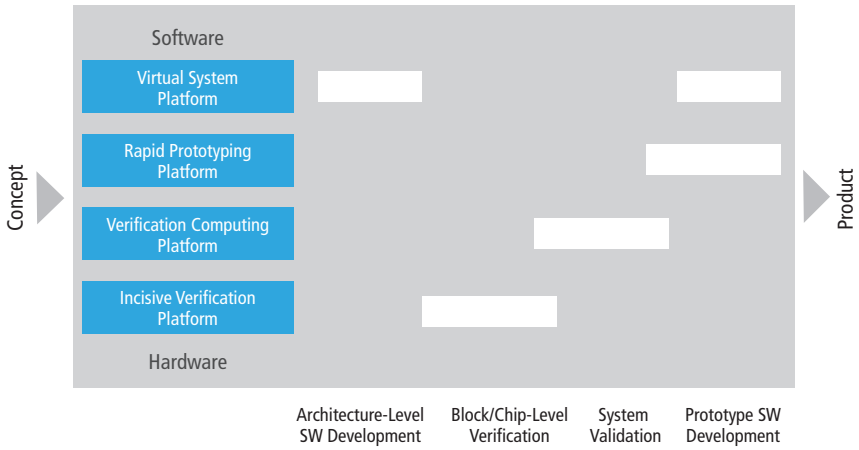

Figure 5: System Development Suite platforms provide hardware/software co-development and integration at different phases of the design flow.

The suite includes the following platforms:

- The Cadence **Virtual System Platform** is a new standards-based (SystemC® TLM) virtual prototyping solution for early software development at the architectural level.
- The Cadence **Incisive® Verification Platform** is a family of verification tools optimized for block-level verification with testbench simulation.
- The **Palladium XP Verification Computing Platform** provides RTL acceleration, emulation and simulation.
- The new Cadence **Rapid Prototyping Platform** consists of FPGA-based prototyping boards supporting up to 30M ASIC gates capacity, and software that provides fast bring-up times.

What is most significant is how these platforms work together. For example, the Virtual System Platform uses the Incisive SystemC simulation kernel, providing a mixed TLM/RTL simulation environment. Incisive and the Verification Computing Platform share compile, debug and run-time environments and can run common accelerated VIP. The FPGA compile engine within the Rapid Prototyping Platform uses the same inputs as the Verification Computing Platform (as well as legacy Palladium products) and uses the same synthesis engine.

Partner and Customer Developments

EDA360 is not just about product and technology announcements—customer adoption and partner relationships are crucial, too. Here are some announcements made by Cadence during the first year of EDA360.

Partner Announcements

- Contributions to TSMC Reference Flow 11 included system-level design and verification, 3D-IC design, and design for manufacturability (DFM), spanning System Realization, SoC Realization, and Silicon Realization (June 2010).
- Cadence collaborated with ARM to develop an optimized System Realization solution for ARM processors that will include interoperable tools, ARM processor and physical IP, and services and methodology (July 2010).
- Cadence extended its System Realization ecosystem partner program (July 2010).

- An exceptionally early collaboration with ARM and Texas Instruments provided tool support for ARM's new Cortex-A15 processor for mobile and consumer applications (Sept. 2010).
- Cadence worked with IBM, GLOBALFOUNDRIES and Samsung to develop a Silicon Realization reference flow (Jan. 2011).
- Cadence and TSMC collaborated to deliver DFM services for advanced process nodes (May 2011).

Customer Announcements

- Chinese foundry SMIC adopted the Cadence Silicon Realization product line for advanced node, low-power designs (Sept. 2010).
- IC design company Open-Silicon taped out a high-performance processor using a Cadence Silicon Realization flow (Nov. 2010).
- High-level synthesis from Cadence helped reduce System Realization time at Fujitsu (Dec. 2010).
- Chinese wireless communications IC provider Spreadtrum Communications used Cadence Silicon Realization products to tape out a 40nm low-power chip (Jan. 2011).
- Japanese design and research consortium STARC deployed Cadence Silicon Realization technology for 32/28nm design (Jan. 2011).
- Broadcom brought Palladium XP into several new lines of business for system-level integration and early hardware/software system validation (Feb. 2011).
- Bosch adopted the holistic constraint-driven design methodology provided by Cadence Virtuoso 6.1 technology (May 2011).

EDA360 into the Future

Within the past year, the concepts behind EDA360 have been widely discussed in the electronics industry—whether the term "EDA360" is used or not. But it's not just talk. And it's not just a vision. As this document shows, Cadence has delivered on the vision with corporate-level changes, product and technology developments, and customer and partner relationships.

As EDA360 enters its second year, Cadence is more committed than ever to delivering industry-leading solutions for System Realization, SoC Realization, and Silicon Realization. With an extensive R&D organization that is now focused on these three Realizations, significant technology innovations will follow. Cadence is also playing a vital role in the standards-based ecosystem that will be required to actualize the EDA360 vision. The benefits of EDA360 will not only extend throughout this ecosystem, but to every consumer of electronic products as well.