# Pegasus Verification System

## Cloud-ready, massively parallel physical signoff

The Cadence® Pegasus™ Verification System is a cloud-ready physical verification signoff solution that enables engineers to deliver advanced-node integrated circuits (ICs) to market faster. The groundbreaking technology delivers up to 10X improved design rule check (DRC) performance on hundreds of CPUs while also reducing turnaround time from days to hours. The Pegasus system's innovative architecture and native cloud processing provides an elastic and flexible computing environment, which enables customers to complete full-chip signoff DRC on advanced-node designs in a matter of hours, helping designers deliver products to market faster. The Pegasus system seamlessly integrates with the industry-standard Cadence Virtuoso® custom/analog platform, the market-leading Cadence Innovus® Implementation System, and mixed-signal flows.

## Advanced-Node DRC Explosion

With the exponential increase in DRC complexity and the number of rules at advanced nodes, market-leading DRC tools are unable to meet the turnaround requirements for advanced-node design schedules. Current full-chip DRC turnaround time is several days, usually on 100 to 200 CPUs. Adding more CPUs does not improve the turnaround time because the scalability of existing tools falls short. Instead, customers use alternative strategies like running the full DRC deck in pieces, where all the sub-decks are run separately over 24 to 30 hours. This is a long time and impacts the designer's productivity. Such slow DRC runtime can impact the project schedule when engineering change orders (ECOs) are applied, leading to delays that can significantly raise the overall cost of the project (Figure 1).

The current market and technology trends have increased the demand for large complex chips, including mixed-signal integration, bringing many challenges. Customers are always looking for viable alternative solutions
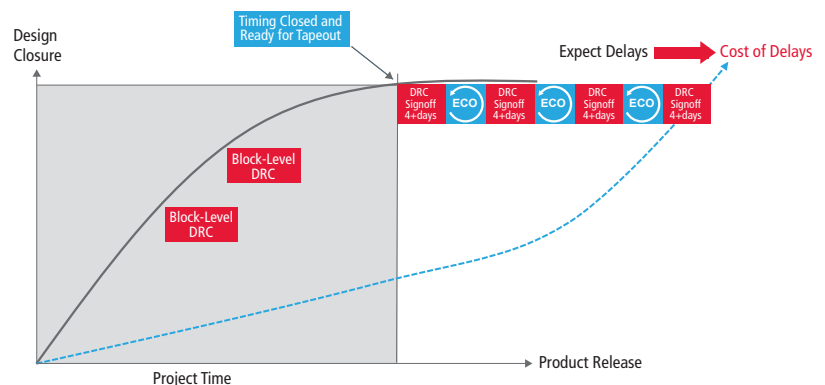


Figure 1: The current DRC turnaround time can take several days, which can impact a project's time to market

for physical verification to not only address current nodes but to enable them to run full-chip DRC efficiently at the most advanced technology nodes. Designers need a fast throughput solution for full-chip DRC, which is seamlessly integrated into the custom and digital design flows. The Pegasus Verification System has demonstrated near-linear scalability on up to 960 CPUs, reducing signoff turnaround time. Now, jobs that previously ran for more than 24 hours can be completed in just a few hours, and users can easily run multiple full-chip DRC signoff jobs during the design process.

## Key Benefits

- Cloud-based platform provides elastic and flexible compute environment for customers facing aggressive time-to-market deadlines

- Massively parallel architecture, gigascale and stream processing provides unprecedented speed and capacity, near-linear scalability, and reduced signoff turnaround time from days to hours

- Efficient use of CPU resources regardless of machine configuration and physical location

- Low transition cost using existing Cadence Physical Verification System (PVS) foundry-certified rule decks

- In-design and signoff DRC from the Virtuoso and Innovus platforms

## Dramatic Turnaround Time Reduction

The Pegasus system provides a massively parallel architecture, and combines a pipelined infrastructure with gigascale and stream processing to deliver near-linear scalability over hundreds of CPUs. As many designs continue to grow in complexity, the Pegasus system can scale to meet the stringent performance and time-to-market goals of customers.

With the Pegasus system, designers can run full-chip DRC on short notice without fear of impacting design schedules. The Pegasus system offers dramatic benefits for all chip designs enabling small blocks to run in minutes over a coffee break, large blocks in hours over a lunch break, and a full-chip job overnight, all resulting in a massive productivity boost. With the Pegasus system, running DRC has now gone from not just necessary but convenient, as well.

## Cloud-Ready Computing

Computing demand fluctuates, resulting in periods where dedicated resources are either underutilized or overloaded. Scaling up and down the hardware according to the application requirements and users' budget makes a cloud-based approach—whether internal or external—a cost-effective, elastic, and flexible option.

The Pegasus system offers native cloud support, and stream processing provides the flexibility for customers to ramp up or down their CPU needs during the design cycle. The Pegasus system's fast turnaround time enables customers to complete more ECOs when needed without impacting the product's time-to-market schedule (Figure 2).
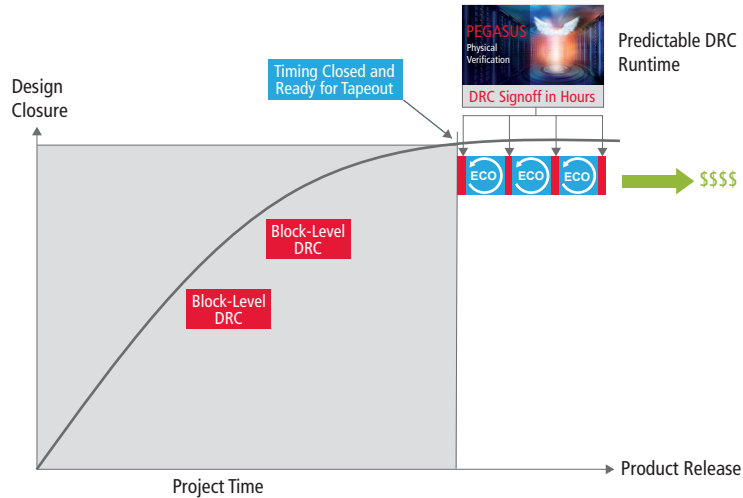


*Figure 2: With the Pegasus system, DRC has gone from being necessary to convenient*

## In-Design and Signoff DRC from the Virtuoso and Innovus Platforms

The Pegasus system seamlessly integrates with the industry-standard Virtuoso custom/analog platform, the market-leading Innovus system, and mixed-signal flows. This integration provides designers with an end-to-end design and signoff physical verification solution integrated with all Cadence tools.

The Pegasus system enables users to complete advanced-node DRC in hours. It uses the existing foundry-certified PVS rule decks, and includes efficient, comprehensive debug tools to reduce debug time and increase productivity. This solution supports advanced-node technologies such as double patterning, triple patterning, quadruple patterning, 3D-IC, FinFET rules, and more.

### Virtuoso/Pegasus Integrated Systems

At advanced nodes, layout engineers need fast DRC to verify that their design is correct. This is where the Virtuoso/Pegasus integrated systems come in, to bridge the gap and improve productivity between the custom implementation and physical verification tools. With the Virtuoso/Pegasus integrated systems, layout teams can achieve productivity improvements of at least 15% at mature nodes and more than 50% at advanced nodes (Figure 3).

### Innovus/Pegasus Integrated Systems

The Pegasus system's integration with the Innovus system enables customers to run various checks during multiple stages of the flow—signoff DRC and multi-patterning decomposition, color-balancing to improve yield, timing-
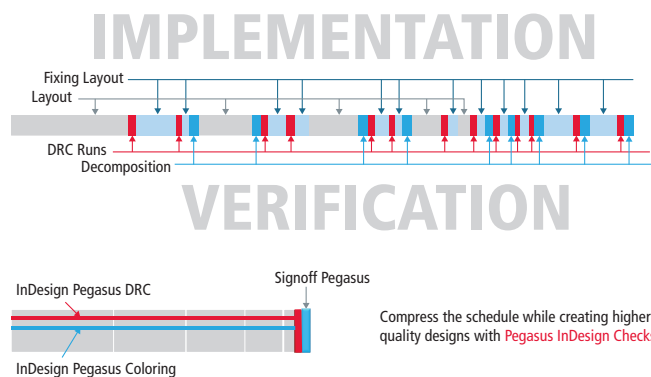


*Figure 3: The Virtuoso/Pegasus integrated systems' DRC check delivers higher quality design—faster!*

aware metal fill to reduce timing closure iterations, incremental DRC, and metal fill during ECOs that improve turnaround time, and full-chip DRC. For mixed-signal flow within the Innovus digital platform, the Pegasus system can interactively verify the design by directly accessing Innovus data and standard cell data from the OpenAccess database. This allows designers to browse DRC errors in the Innovus system or in the standalone Pegasus QuickView and view the error.

At advanced nodes, the metal fill rules have become more complex and the previous approach of estimating approximate dummy fill in place and route and then using foundry-qualified signoff fill isn't adequate to meet the mandatory density rules. The addition of metal shapes in a design impacts parasitic extraction, timing analysis, and signal integrity, and improper implementation causes several iterations between place and route and signoff timing analysis.

With the Innovus/Pegasus integrated systems, the metal fill flow uses the foundry-certified PVS metal fill rule decks and offers a correct-by-construction, timing-aware flow. Unlike traditional flows where full-chip metal is run for ECOs, the Innovus/Pegasus integrated systems' metal fill flow offers between 50% to 80% runtime in metal fill via incremental metal fill using the Pegasus system and is timing aware (Figure 4).

## Low Transition Cost

The Pegasus system uses the existing foundry-certified Cadence PVS rule decks. This allows users to leverage their investments in PVS rule decks and infrastructure with less effort for translation or scripts. Rule decks are in the physical verification language (PVL)
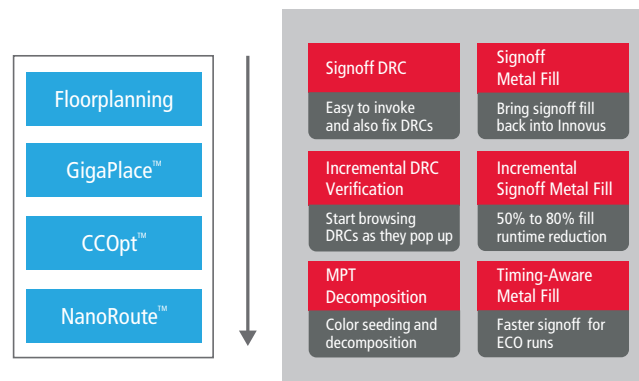


Figure 4: Use the Pegasus system to seamlessly run DRC, timing-aware fill, and color-balancing to improve yield, with automated DRC fixing in the Innovus system.

format and execute natively on the Pegasus system, which reports design errors in an intuitive, predictable, and familiar way. This greatly accelerates tool and flow validation and integration, allowing customers to achieve 100% accurate results with a minimal learning curve.

## Pegasus QuickView Signoff Data Analysis Environment

The Pegasus QuickView Signoff Data Analysis Environment tightly integrates the Pegasus system with QuickView, the industry's production-proven, full-chip, high-performance, high-capacity, data-viewing, and standalone chip-finishing system that supports multiple formats of design, layout, and manufacturing data. The Pegasus QuickView Signoff Data Analysis Environment loads large layouts (GDSII, OASIS, LEF/DEF, and manufacturing formats) in seconds, and provides a rich set of debugging features, including net connectivity tracing, visualization, overlay, and GDSII/OASIS editing.

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training

- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom

- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training