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IN2P3 and Cadence

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Daniel Charlet, Design Engineer, IN2P3

The Customer

The National Institute of Nuclear and Particle Physics (IN2P3) of the Centre National de la Recherche Scientifique (CNRS) promotes and unifies research activities in nuclear, particle, and astroparticle physics. Founded in 1971, IN2P3, working in partnership with CEA (French Alternative Energies and Atomic Energy Commission), coordinates programs in these fields on behalf of CNRS and universities.

To perform its scientific explorations, IN2P3 relies on a variety of very large instruments and infrastructures, including particle accelerators and detectors that are space-based, ground-based, or even undersea.

In particular, scientists at IN2P3 utilize the world's largest and highest energy particle accelerator, the Large Hadron Collider (LHC), located close to Geneva, Switzerland. The collider, which consists of a circular accelerator 27km long with six detectors along this ring, was built by the European Organization for Nuclear Research (CERN) to provide physicists with a tool to test the predictions of different particle physics and high-energy physics theories.

Because of detector complexity (each consists of millions of channels) and the high performance required to process huge amounts of data in real time, FPGAs are at the heart of most of the electronics systems developed to operate the system. Recently, two of IN2P3's research teams involved in the readout and supervision system of the LHCb experiment on the LHC developed boards with large FPGAs.

Business Challenge

- Enhance ability to meet aggressive deadlines for particle physics research projects

Design Challenges

- Automate aspects of FPGA board design, including pin placement and routing schemes
- Quickly select the optimal FPGA package and pin count for the design
- Quickly determine the right FPGA configuration and component setup for the design

Cadence Solutions

- Allegro FPGA System Planner
- Allegro Design Authoring
- Allegro PCB Designer
- Allegro PCB SI

Results

- Saved one to two months based on FPGA interconnect density on manual FPGA design-in effort for initial design
- Made late changes to the design easily and in hours vs. weeks
- Reduced design iterations and, as a result, costs
- Saved one month of project time due to co-design development ability

The Challenge

Daniel Charlet, an IN2P3 design engineer, is responsible for building and managing a FPGA-based board that realizes the interface between a PCI Express bus and a specific radiation-hardened link based on a custom protocol. His board consists of a transceiver-based 28nm Altera FPGA with SSRAM, an AMC standard backplane connector, a high-density HSMC connector, and multiple interfaces providing connections to the specific link. Generating register-transfer level (RTL) code from the FPGA, determining pin placement and routing schemes, and managing other architectural tasks were previously manual processes. Over time, such manual processes proved to be too time-consuming, given that the researchers need to finish the projects in shorter timeframes. Charlet needed to find a more efficient way to implement his FPGA-based designs.

Jean-Pierre Cachemiche, an IN2P3 project manager, faced a similar challenge. He has built a FPGA-based set of boards that concatenates in real time data coming from the same collision (40 million collisions occur per second) and sends it toward a data processing farm consisting of several hundred computers. The full system should contain between 600 and 800 of these boards. Such experiments have lifetimes of 10 to 15 years, and their complexity requires several years of test and integration before they are deemed operational. The challenge is to choose the most up-to-date technology to achieve the maximum performance without taking risks by redesigning a new board when it is too late in the process. Clearly, design speed is critical.

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The Solution

IN2P3 is no stranger to Cadence® tools, having used Cadence Allegro® products—including Allegro Design Authoring, Allegro PCB Designer, and Allegro PCB SI—for some 20 years in its labs. Charlet turned to Cadence Allegro FPGA System Planner to manage the FPGA-PCB co-design process and create the ideal correct-by-construction pin assignment for his design. Allegro FPGA System Planner provides automatic pin assignment synthesis, so users can quickly create initial pin assignments for FPGA placement on the PCB, without having to endure a slower, and potentially error-prone, manual process.

"I like that Allegro FPGA System Planner is well integrated with the rest of the Allegro products," said Charlet. "I also appreciate the high level of abstraction that Allegro FPGA System Planner provides. With a top view of our design, we get a clear picture of the relative placement of the FPGA with other components on our board, and we can quickly scale between smaller and larger FPGAs."

As a first-time user of the tool, Charlet experienced the learning curve that is natural of any such situation. He noted that the support from, and collaboration with, the Cadence team helped make the deployment of Allegro FPGA System Planner a smooth one.

As for Cachemiche, he selected Allegro FPGA System Planner to quickly assess the feasibility of proposed FPGA board layouts, before committing to the layouts. "Before, we had to run the full board design chain before we could see if there would be enough room for all of our components. Through a manual process, we would have had to spend a lot of time optimizing connections of this 1,920-pin FPGA and the layout of quite sensitive 10 Gb/s connections. With Allegro FPGA System Planner, we can quickly ensure that pin placement and routing are correct. We can also change FPGAs and other components very quickly in our design, without having to do a time-consuming manual schematic update effort."

Using Allegro FPGA System Planner, Cachemiche and his team conducted experiments with different orientations of the parts on their board, to determine which configuration was best from a routing perspective. "Working with the PCB designer, who used Allegro PCB Designer for constraints-driven PCB design and Allegro PCB SI for advanced interconnect modeling, we were able to efficiently communicate placement and pin assignment goals and issues and, ultimately, converge on a solution much faster than with our old methods," explained Cachemiche.

With the old methods, the FPGA and PCB design teams worked iteratively. "Now we can co-design because we can reverse the design flow —we start by placing components, and we can begin routing before we have a final FPGA design," said Cachemiche. "Once we are reassured on our layout, we can develop a schematic in a couple of minutes, establish the pin placement for the FPGA, and then compile. Finally, we complete the process with a deep verification of the automatically generated schematics."

The Benefits

Both Charlet and Cachemiche anticipate substantial time savings in future FPGA deployments, by automating manual design processes with Allegro FPGA System Planner. With a floorplan view of their boards, the engineers can easily place components in their systems and specify connectivity between them. Doing so, they can shorten the overall design cycle and, as a result, lower costs by eliminating unnecessary physical

design iterations—a scenario that's unavoidable with manual approaches. What's more, the teams are equipped to make late changes to their designs in hours, rather than the weeks it would take if they were using manual processes.

Since pin assignment is optimized for routing at the start, IN2P3 anticipates requiring fewer layers on its FPGA-based boards, which translates into less expensive boards.

Said Charlet, "Instead of starting with FPGA code and forcing pin assignments onto the schematic engineer and FPGA designer, we can plan pin assignments first using Allegro FPGA System Planner and then move to RTL code—true FPGA and PCB co-design. With pin coding established at an abstract level, we can save one or two months of work. Considering that our FPGA-based design has around 800 pins, the impact is substantial."

Summary and Future Plans

A tool like Allegro FPGA System Planner provides the IN2P3 teams with the flexibility to more efficiently upgrade or reconfigure their FPGA-based systems, without having to start from scratch. They can reassess pin assignments and connectivity in just a couple of hours, compared to the upwards of 10 hours if they had to do this manually on their particular designs.

The teams expect to build on their expertise with the Allegro tool to gain more efficiencies with future FPGA designs.